What is claimed is:

1. A dual level flash memory cell comprising:

a p-type substrate;

a first active region and a second active region formed in the substrate;

a first insulator dielectric formed on the first active region, the second active region, and the substrate, wherein the first insulator dielectric is operable to store electrons for first and second bits of information;

a first poly layer formed on the first insulator dielectric;

a second insulator dielectric formed on the first poly layer, wherein the second insulator dielectric is operable to store electrons for a third bit of information; and

a second poly layer formed on the second insulator dielectric.

2. The memory cell of claim 1, wherein the first insulator dielectric is comprised of a bottom dielectric, a narrow bandgap material formed on the bottom dielectric, and a top dielectric formed on the narrow bandgap material.

3. The memory cell of claim 2, wherein the bottom dielectric is comprised of silicon dioxide, the top dielectric is comprised of silicon dioxide, and the narrow bandgap material is comprised of nitride.

4. The memory cell of claim 2, wherein the bottom dielectric is comprised of silicon dioxide, the top dielectric is comprised of silicon dioxide, and the narrow bandgap material is comprised of silicon-germanium.

5. The memory cell of claim 2, wherein the bottom dielectric is relatively thin and the top dielectric is relatively thick.

6. The memory cell of claim 2, wherein the bottom dielectric is relatively thick and the top dielectric is relatively thin.

7. The memory cell of claim 1, further comprising a vertical structure of the first insulator dielectric to facilitate scaling.

8. The memory cell of claim 7, wherein the vertical structure is V-shaped.

9. The memory cell of claim 7, wherein the vertical structure is U-shaped.

10. The memory cell of claim 1, further comprising:

a third insulator dielectric formed on the second poly layer, wherein the third insulator dielectric is operable to store electrons for a fourth bit of information; and

a third poly layer formed on the third insulator dielectric.

11. The memory cell of claim 10, further comprising one or more additional pairs of insulator dielectrics/poly layers, wherein each pair comprises:

an additional insulator dielectric formed on the memory cell; and

an additionally poly layer formed on the additionally insulator dielectric.

12. The memory cell of claim 1, wherein the third bit of information is operable to be read by applying a read voltage to the second poly layer, wherein the read voltage is a function of values of the first and the second bits of information.

13. The memory cell of claim 1, wherein the first poly layer and the second poly layer are comprised of metal.

14. A method of fabricating a dual level memory cell comprising:

forming a first active region and a second active region in a substrate;

forming a first insulator dielectric on the substrate;

forming a first poly layer on the first insulator dielectric;

forming a second insulator dielectric on at least a portion of the first poly layer; and

forming a second poly layer on the second insulator dielectric.

15. The method of claim 14, further comprising forming a trench in the substrate between the first active region and the second active region prior to forming the first insulator dielectric such that a vertical structure is formed by the first insulator dielectric.

16. The method of claim 15, wherein the vertical structure is V-shaped.

17. The method of claim 14, wherein the second poly layer is formed orthogonal to the first poly layer.

18. The method of claim 14, wherein forming the first insulator dielectric comprises forming a first oxide layer on the substrate, forming nitride on the first oxide layer, and forming a second oxide layer on the nitride.

19. The method of claim 14, wherein the first active region and the second active region are formed to be n-type and the substrate is p-type.

20. A method of programming a dual level memory cell having a first active region, a second active region, a first insulator dielectric, a first gate, a second insulator dielectric, and a second gate, the method comprising:

programming a first lower bit in a first mode of operation;

programming a second lower bit in a second mode of operation; and

programming an upper bit by connecting a second gate to ground and applying a negative voltage to a first gate.

21. The method of claim 20, wherein programming the first lower bit comprises:

operating the first active region as a source;

operating the second active region as a drain; and

applying a program voltage to the first gate.

22. The method of claim 21, wherein programming the second lower bit comprises:

operating the first active region as a drain;

operating the second active region as a source; and

applying a program voltage to the first gate.

23. A method of erasing a dual level memory cell having a first active region, a second active region, a first insulator dielectric, a first gate, a second insulator dielectric, and a second gate, the method comprising:

erasing a first lower bit by applying a relatively high voltage to an acting source and applying a negative voltage to the first gate while floating an acting drain, wherein the acting source is the first active region and the acting drain is the second active region;

erasing a second lower bit by applying a relatively high voltage to an acting source and applying a negative voltage to the first gate while floating an acting drain; wherein the acting drain is the first active region and the acting source is the second active region; and

erasing an upper bit by applying a negative voltage to the second gate and connecting the first gate to ground.

24. The method of claim 23, wherein erasing the upper bit comprises releasing trapped electrons form the second insulator dielectric to the first gate.

25. A method of reading a dual level memory cell having a first active region, a second active region, a first insulator dielectric, a first gate, a second insulator dielectric, and a second gate, the method comprising:

reading a first lower bit by applying a threshold voltage to the first gate and detecting current flow in a first mode of operation, wherein the first active region is an acting source and the second active region is an acting drain;

reading a second lower bit by applying the threshold voltage to the first gate and detecting current flow in a second mode of operation, wherein the first active region is an acting drain and the second active region is an acting source;

determining a suitable read voltage for an upper bit according to the read first and second lower bits; and

reading the upper bit by applying the suitable read voltage to the second gate while permitting the first gate to float.

26. The method of claim 25, wherein the read voltage is determined by selecting one of a set number of voltages corresponding to the read first and second lower bits.